

APPENDIX A
"CLEAN" VERSION OF EACH PARAGRAPH/SECTION/CLAIM
37 C.F.R. § 1.121(b)(ii) AND (c)(i)

SPECIFICATION:

Replacement for the paragraph beginning on page 5, line 12:

R1
Consequently, the device of Figure 3 has the same breakdown voltage as that of Figure 2 since the area under the curve in Figure 4 is about the same as that of Figure 2. However, the on-resistance is reduced because of the total reduced epi depth and the reduced resistivity in the first epi layer. These resistance comparisons are listed directly on Figure 5, comparing the total on-resistances of the single and dual epi layer embodiments.

CLAIMS (with indication of amended or new):

R2
1. (Five Times Amended) A semiconductor device comprising, in combination, a silicon substrate having a first and second surface; a first layer disposed on said first surface and having impurities of the n or p conductivity type uniformly distributed throughout the volume of said first layer; a second layer disposed on said first layer; said second layer having impurities of the same type as those in said first layer uniformly distributed therethrough and having a substantially uniform resistivity; the concentration of impurities in said second layer being greater than the concentration of impurities in said first layer; and a plurality of diffusions of a conductivity type opposite to that of said second layer distributed uniformly into the surface of said second layer and defining p-n junctions therein; said plurality of diffusions being spaced from one another and each having a depth that is less than the thickness of said second layer whereby each diffusion is wholly contained within said second layer.